

CAN1630G SPDT Switch Datasheet

Rev 1.2 April, 2019

This datasheet is intended for customer's evaluation and application of the CAN1630G device. Under no circumstances it should be circulated outside the customer's company. This datasheet is preliminary and CanaanTek reserves the right to modify and to improve the data.





PRODUCT DESCRIPTION

CAN1630G is a single pole, dual-throw (SPDT) LTE MMMB transmit/receive switch. Switching is controlled by an integrated GPIO interface with a single control pin. Depending on the logic voltage level applied to the logic control pin, the antenna port is connected to one of the switched RF ports (RF1 or RF2) through a low insertion loss path, while the path between the antenna port and the other RF port is in a high isolation high impedance state.

No external DC blocking capacitors are required as

lon5/063/100/290/avol/(40074)3755.86 Tm0 g0 G[(2)]TJET EMC /Span & Rlen-

The CAN1630G is manufactured using a

state-of-the-art Silicon-On-Insulator (SOI) process and

is provided in a compact 1.1 x 0.7 x 0.45 mm, 6-pin

surface mount Dual Flat No-Lead (DFN) package.

A faidetional block diagram is solver transm ac7 44/Lang (en-US)>> BDC q 12/Lang (efy)18()- T08871 0 nd iSapan × BD



Table 1. CAN1630G Signal Descriptions

Pin#	Name	Description	Pin#	Name	Description
1	RF2	RF I/O, throw 2	4	VDD	Voltage supply
2	GND	Ground	5	ANT	RF I/O, switch pole
3	RF1	RF I/O, throw 1	6	VCTL ¹	Switch control line

Note 1: If VDD is powered down, VCTL should be low level.

Electrical and Mechanical Specifications

The absolute maximum ratings of the CAN1630G are provided in Table 2.

Electrical specifications are provided in Table 3.

The state of the CAN1630G is determined by the logic provided in Table 4.

Table 2. CAN1630G Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Supply voltage	VDD	1.6	5.0	V
Digital control voltage	VCTL	0.0	3.3	V
RF input power	PIN		35	dBm
Supply ripple	V _{PP}		20	mV_{PP}
Operating temperature	T _{OP}	-40	+85	°C
Storage temperature	Tstg	-55	+150	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to

debiee2with only one parameter set at the limit and all other parameters set at or 1 0 0f3/F2 9.96 Tf1 0 0 1 dr369.850.45 69.384



Table 3. CAN1630G Electrical Specifications (Note 1)

$(V_{\text{DD}} = 2.85 \text{V}, \, T_{\text{OP}} = +27 \,\, ^{\circ}\text{C}, \, Characteristic \, Impedance \, [Z_{\text{O}}] = 50 \quad , \, Unless \, Otherwise \, Specified)$

Parameter	Symbol	Test Condition	Min	Typical	Max	Units	
DC Specifications							
Supply voltage	VDD		1.60	2.85	4.5	V	
Control voltage:							
Low	VCTL_L		0	0	0.40	V	
High	VCTL_H		1.20	1.80	VDD	V	
Current on VCTL pin	I_CTL				5	μA	
Supply ourrept	IDD	VDD = 2.85 V,		25	60		
Supply current		VCTL = VCTL_H			60	μΑ	
		Measured from VCTL_HIGH minimum or					
PE path switching time	tSW	VCTL_LOW		1	2		
KF path switching time		maximum to RF output power ± 1 dB (Note 2),		I	5	μο	
		$PIN = +26 \text{ dBm}, \text{T}_{OP} = -10 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}.$					
RF Specifications							
Insertion loss (PE1 or PE2	IL	0.1 to 1.0 GHz		0.30	0.50	dB	
to ANT nin)		1.0 to 2.2 GHz		0.35	0.55	dB	
		2.2 to 2.7 GHz		0.37	0.60	dB	
Isolation from any active	lso	0.1 to 1.0 GHz	30	35		dB	
nort to any other port		1.0 to 2.2 GHz	28	33		dB	
port to any other port		2.2 to 2.7 GHz	20	25		dB	
0.1 dB Input Compression	P0.1dB	VDD=2.85V		34.5		dBm	
Point							
Voltage Standing Wave	VSWR	Referenced to 50 ,0.1 to 2.7 GHz		1 0.1	1 5.1		
Ratio, all ports				1.2.1	1.5.1	-	
Hermonia DE1 or DE2 to	Harm	fo = 0.1 to 2.7 GHz,					
		PIN = +26 dBm,		-65	-55	dBm	
		VSWR = 2.5:1					

Note 1:







Table 4. CAN1630G Truth Table

State	Active Path	VCTL (Pin 6)
0		





Timing Requirements

It is important that the user adheres to the correct timing sequences in order to avoid leakage power consumption.

 VDD and VCTL cannot be powered on and off independently from one another. During power on sequence, the user must power up VDD first, then power up VCTL. During power off sequence, the user must power off VCTL first, then power off VDD. In the state of VDD=OFF(0 V) and VCTL=ON(1.8V), it may cause leakage power consumption as ESD protection circuit inside the switch.



Figure 4. Allowable Power On Sequences

2. VDD and VCTL must be on for a minimum of 15us before applying RF power.



Figure 5. RF Power-Up Detail





Switch Model for RF ON/OFF state

Please note that Switch model for RF1 ON and RF2 ON as the following.

Refer to the Figure 6, when RF1 ON, RF1 port and ANT port will be connected directly in short circuit, while RF2 port will be connected to the Ground through internal switch, so it should avoid DC level applied on RF2 port.

Refer to the Figure 7, it's vise versa for RF2 ON.



Figure 6. Switch model with RF1 ON









Package Dimensions

Package dimensions for the CAN1630G are shown in Figure 5.



	MILLMETER		
SYMBOL	MIN	NOR	MAX
А	0.41	0.45	0.50
A1			

Figure 8. CAN1630G Package Dimensions







PCB Metal, Solder, and Stencil Patterns





Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE CAN1630G is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.





Revision History

Revision	Comments		
Rev1.0	First Draft		
Rev 1.1	Add PCB Metal, Solder, and Stencil Patterns		
Rev 1.2 Add timing requirement, RF ON/OFF model description and Typo correct			