

Change Summary

CHANGES

No.	Applicable Section	Description	Page(s)
1	Electrical Characteristic	Updated	5-8
2	General description	Updated	2
3	Functional description	Updated	10,11,13,15
4	Typical application schematic	Updated	28
5			
6			
7			
8			

REVISION HISTORY

Revision No.	Description of change	Release Date
0.5	Initial release	2017/12/05
0.7	Updated #1	2018/03/12
0.71	The changes are listed above from #2 to #3,#4	2018/05/09



I²C Controlled 3A Fully Integrated 1 Cell Li-Ion Battery NVDC Charger with MPPT control for Solar Panel

FEATURES

- High accuracy switched mode 1 cell Li-lon charger with integrated synchronous switching MOSFETs
- Support Intel NVDC topology
- Support Quick Charge, VBUS input voltage up to 14V
- Support VINDPM mode to set the MPPT voltage using for solar panel power
- Input current optimization function to identify the maximum input power to not overload
- Dynamically allocates USB input power including input voltage regulation and input current limit to adapt all kinds of adapter
- Constant ripple current (CRC) control and no external loop compensation
- Integrated charging sensing resistor and input current sensing resistor
- Integrated bootstrap diode
- Support USB 2.0, 3.0 USB Standards and higher voltage adapter
- Setting charging current from 0A to 3A
- Integrated 15mΩ battery discharge MOSFET up to 9A pulse discharge current to get highest battery discharging efficiency
- I²C programmable battery path impedance compensation to accelerate charge time
- Up 93% charge efficiency at 2A and 91% at 3A
- I²C setting and battery charge management
 - ±0.5% voltage mode accuracy
 - ±5% current mode accuracy
 - ±3% VBUS input voltage limit accuracy
- 100mA to 3.25A input current limit
- VBUS UVLO and Over-Voltage Protection, VSYS Over-Voltage Protection
- Power MOSFETs Over-Current Protection
- Support shipping mode
- · Joint Power Supply when system over load
- Support autonomous battery charging process without I²C communication
- Provides telemetry and charging status indication information via I²C(voltage, temperature, current)
- Interrupt output IRQ to host
- Thermal regulation and Over Temperature Protection
- Charger safety timer
- Low battery current dissipation when only battery present
- Lead free and RoHS Compliant

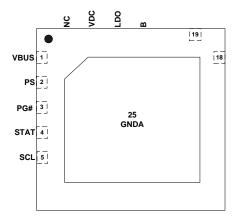
APPLICATIONS

- · Shared bike
- Cell Phone
- Other Solar Panel devices

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ1C82	-40°C to 125°C	QFN24, 4mmx4mm

PIN DIAGRAM





GENERAL DESCRIPTION

OZ1C82 is an I²C controlled power management IC for single cell Lilon or Li-polymer battery systems in a wide input range of Solar panel powered devices, like shared bike, power bank or other portable device.

OZ1C82 supports all kinds of input sources; the voltage range is from 3.9V up to 14V in operation, which is very suitable for solar panel application since the solar panel voltage is variable with different weather ere



BLOCK DIAGRAM

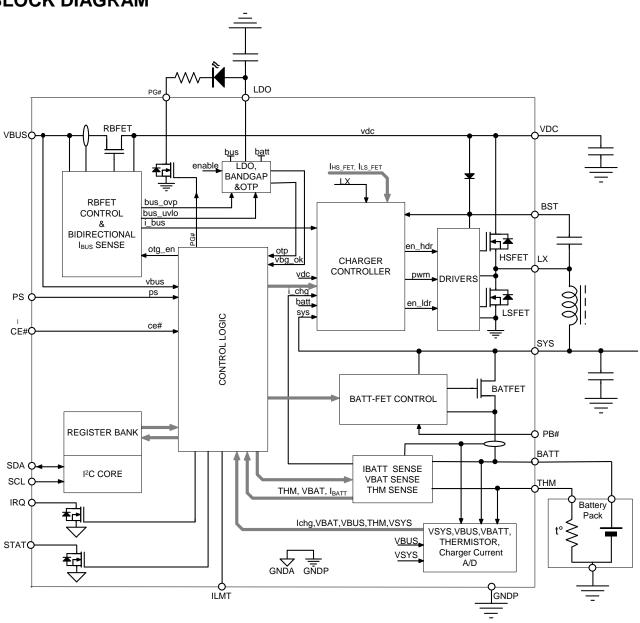


Figure 1: OZ1C82 Block Diagram



PIN DESCRIPTION

Pin	Name	I/O	Туре	Description
1	VBUS	Р	Power	Solar Panel or USB, adapter input, a 1uF ceramic capacitor should be placed from VBUS to PGND as close as to the IC.
2	PS	I	Digital	Selects default I _{BUS} limit when BUS power becomes available; High indicates a USB source and low indicates an adapter source
3	PG#	0	Digital	Open drain active low power good indicator Connect to the pull-up rail through a 10k resistor
4	STAT	0	Digital	Open drain output signalizing charging status with a 10kΩ pull up resistor: - charging - consistently low - charging legally stopped or charger disabled- consistently high - charging stopped by any fault condition – blinking with 1Hz
5	SCL		Digital	Serial I ² C Clock signal; connect by a resistor to pull-up rail.
6	SDA	I/O	Digital	Serial I ² C Data signal; connect by a resistor to pull-up rail.
7	IRQ	0	Digital	Interrupt request output pin – open drain and low pulse active Connect to the pull-up rail through a 10k resistor
8	OTG	ı	Digital	Connected to ground.
9	CE#		Digital	Charge Enable pin. Active low
10	ILMT	I	Analog	Connected to ground.
11	ТНМ	I	Analog	Input of battery temperature detection circuitry. Connect a NTC resistor to this pin. Program temperature with a resistor divider from LDO to THM to ground. When THM is out of range, charge suspends.
12	PB#	I	Digital	BATFET ON/OFF control pin. When PB# is pull low for t _{SHIPMODE} to turn on BATFET when BATFET is off in shipping mode. When PB# is pull low for t _{PB_RST} (15s typical) without VBUS plugging in, BATFET will turn off then on to reset system.
13	VBAT	Р	Power	Battery charger output and battery voltage sense pin. Connect to battery cell. The internal BATFET is connected between VBAT
14	VBAT	Р	Power	and VSYS, connect a 10uF capacitor closely to VBAT pin
15	VSYS	Р	Power	System voltage output.
16	VSYS	Р	Power	Connect a 20uF capacitor closely to VSYS pin
17	GNDP	Р	Power	Ground for Power section
18	GNDP	Р	Power	Ordana for Fower Section
19	LX	Р	Power	Switching Node Connection
20	LX	Р	Power	
21	BST	Р	Power	Positive supply for the high side driver. A 0.047µF capacitor should be placed between BST and LX.
22	LDO	Р	Power	Power supply for the internal analog circuit. Bypass to ground by 4.7µF ceramic capacitor placed as close as possible to the pins
23	VDC	Р	Power	Charger input node. A 10µF capacitor is needed from this pin to GNDP.
24	NC	-	-	NC



ABSOLUTE MAXIMUM RATINGS

VBUS, VDC to GNDP	0.3V to +18V
LDO, VSYS, VBAT to GNDP	
LX referred to GNDP and VDC	GNDP-0.5V to VDC+0.5V
PS, STAT, PG#, CE#, PB#, THM, IRQ, ILMT to GNDP	0.3V to LDO+0.3V
BST referred to LX	0.3V to +7V
SCL, SDA to GNDP	0.5V to +7V
Maximum Operating Junction temperature	+125°C
Storage temperature range	55°C to +150°C

NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

VBUS, VDC to GNDP	3.9V to 14V
SDA, SCL, PS, STAT, PG#, CE#, PB#, THM, IRQ, ILMT	
VSYS, VBAT	
Operating temperature range (ambient)	

ELECTRICAL CHARACTERISTICS

 $V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} > V_{SLEEP}$, $T_J = -40^{\circ}C$ to +125°C and $T_J = 25^{\circ}C$ for typical values (unless otherwise noted)

	PARAMETER	TEST	MIN	TYP	MAX	UNITS
QUIESCENT	CURRENTS					
I _{VBUS}		VVBUS = 5 V, High-Z mode, no battery, battery monitor disabled		15	30	μΑ
		VVBUS = 12V, High-Z mode, no battery, battery monitor disabled		30	50	μΑ
	Input supply current (VBUS)	VVBUS > VUVLO, VVBUS > VBAT, converter not switching		1.5	3	mA
		VVBUS > VUVLO, VVBUS > VBAT, converter switching, VBAT=3.2V, ISYS=0A	3			mA
		VvBus > VuvLo, VvBus > VBAT, converter switching, VBAT=3.8V, Isys=0A		3		mA
VBUS/BAT P	OWER UP		•			
V _{VBUS_OP}	VBUS operating range		3.9		14	V
V _{VBUS_UVLOZ}	VBUS for active I ² C, no battery	V _{VBUS} rising	3.6			V
V _{SLEEP_F}	Sleep mode falling threshold	V _{VBUS} falling, V _{VBUS-VBAT}	25	65	120	mV
V _{SLEEP_R}	Sleep mode rising threshold	V _{VBUS} rising, V _{VBUS-VBAT}	130	250	370	mV
V _{ACOV}	VBUS over-voltage rising threshold	V _{VBUS} rising	14		15	V
	VBUS over-voltage falling threshold	V _{VBUS} falling	13.5		14.5	
V_{BAT_UVLOZ}	Battery for active I ² C, no VBUS	V _{BAT} rising	2.3		•	V



ELECTRICAL CHARACTERISTICS (Continued)

 $V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} > V_{SLEEP}$, $T_J = -40^{\circ}C$ to +125°C and $T_J = 25^{\circ}C$ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN TYP	MAX	UNIT
R _{ON(HSFET)}	Internal top switching MOSFET on	T _J = -40°C - 85°C	22	mΩ	
NON(HOPET)	resistance between VDC and LX	T _J = -40°C – 125°C	22		22
	Internal bottom switching	T _J = -40°C - 85°C	24		0
R _{ON(LSFET)}	MOSFET on-resistance between LX and PGND	T _J = -40°C - 125°C	24		mΩ
V _{FWD}	BATFET forward voltage in supplement mode	Battery discharge current 10mA	30	•	•



ELECTRICAL CHARACTERISTICS (Continued)

 $V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} > V_{SLEEP}$, $T_J = -40^{\circ}C$ to +125°C and $T_J = 25^{\circ}C$ for typical values (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic I/O p	in Characteristics (CE#,PS,PB#)					
V _{IH}	Input high threshold level		1.3			V
V_{IL}	Input low threshold level				0.4	V
I _{IN_BIAS}	High level leakage current	Pull-up rail 1.8V			1	uA
		Battery only mode		VBAT		
$V_{PB\#}$	Inter PB# pull-up	V _{VBUS} =9V		5.1		V
		V _{VBUS} =5V		4.8		
R _{PB#}	Internal PB# pull-up resistance			1		ΜΩ
Logic I/O p	in Characteristics (IRQ,STAT,PG#)					
V _{OL}	Output low threshold level	Sink current=5mA			0.4	V
I _{OUT_BIAS}	High level leakage current	Pull-up rail 1.8V			1	uA
I ² C Interfac	e (SCL,SDA)					
V _{IH}	Input high threshold level, SCL and SDA	Pull-up rail 1.8V	1.3			V
V _{IL}	Input low threshold level, SCL and SDA	Pull-up rail 1.8V			0.4	V
V _{OL}	Output low voltage level	Sink current=5mA			0.4	V
I _{BIAS}	High level leakage current	Pull-up rail 1.8V			1	uA

Timing Requirements

	PARAMETER	TEST CONDITIONS	MIN TYP MAX	UNIT
I ² C Interface	(SCL,SDA)			
fscL	SCL clock frequency		400 ^{Note 1}	kHz
Battery Over	r-voltage Protection		•	
t _{BATOVP}	Battery over-voltage deglitch time to disable charge		1	us
Battery Chai	rger			
trechg	Recharge deglitch time		20 ^{Note 1}	ms
Battery mon	itor			
t _{CONV}	Conversion time	CONV_RATE(REG02[6])=1	1000 ^{Note 1}	ms
PB# and Shi	pping Timing			
t _{SHIPMODE}	PB# low time to turn on BATFET and exit ship mode	T _J =-10°C-60°C	1.75 ^{Note 1}	sec
t _{QON_RST}	PB# low time to enable full system reset	T _J =-10°C-60°C	15 ^{Note 1}	sec
t _{BATFET_RST}	BATFET off time during full system reset	T _J =-10°C-60°C	450 ^{Note 1}	ms
t _{SM_DLY}	Enter ship mode delay	T _J =-10°C-60°C	12.5 ^{Note 1}	sec
Digital Clock	k and Watchdog Timer			
f _{LPDIG}	Digital low power clock	LDO disabled	30	kHz
f _{DIG}	Digital clock	LDO enabled	1000	kHz
t _{WDT}	Watchdog time	Watchdog (REG07[5:4]=01),LDO enabled	40 ^{Note 1}	sec

Note 1: all the items with Note 1



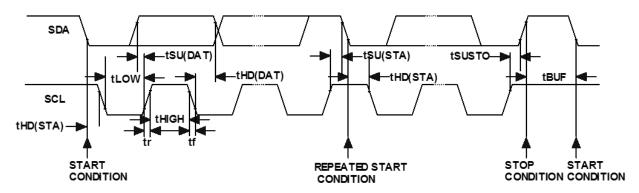


Figure 2:1²C Timing Diagram



FUNCTIONAL DESCRIPTION

Device power-on-reset (POR)

The internal bias circuit is powered from the higher voltage between VBUS and VBAT. When VBUS rises above VVBUS_UVLOZ or VBAT rises above VVBUS_UVLOZ or VBAT rises above VVBUS_UVLOZ, 6th@225tepp [(W)4706.5 E42 82en-U\$924 TJ E31Tq824 3 E31T42s comparator, battery depletion comparator and BATFET driver are active. I²C interface is ready for communication and all registers are reset to default value. The host can access all the registers after POR.

Device powered up from battery without input source

WRen only battery is present and the battery voltage is above the depletion threshold (V_{BAT_DPLZ}), the BATFET turns on and connects battery to system. The LDO stays off to minimize the quiescent current. The low $R_{DS(ON)}$ of BATFET and low quiescent current on VBAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharging current through BATFET.

When the system is overloaded or shorted(IBAT>I



forced to the lower of 100mA or ILIM pin. After the system rises above 2.2V, the device limits the input current to the lower value of ILIM pin and IINLIM register. In order to improve the light–load efficiency, the device enters skip mode at light load.

Input current optimizer (ICO)

OZ1C82 provides input current optimizer (ICO) to indentify maximum power point without overload the input source. The algorithm automatically identifies maximum input current limit of power source without entering VINDPM to avoid input source overload.

The feature is disabled by default (ICO_EN=0) and can be enabled by setting ICO_EN bit to 1. After the input source is detected, ICO runs automatically when ICO_EN bit is set. The algorithm can also be forced to execute by setting FORCE_ICO bit regardless of input source type



For safe operation, the host should set the maximum allowed regulation voltage register and the minimum resistance compensation.

JEITA guideline compliance in charge mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charging current and high charging voltage at certain low and high temperature ranges.

The OZ1C82 continuously monitors battery temperature by measuring the voltage between the THM pin and ground, typically determined by a negative temperature coefficient thermistor (NTC) and an external voltage divider. The OZ1C82 compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle; the voltage on THM pin must be within the VT1 to VT5 thresholds. If THM voltage exceeds the T1–T5 range, the controller suspends charging and the LED

connecting to ST pin will blinks on andefd withd2Hz1(HM)2[()] TJETBT1 0 0 1 5723.464.83 Tmf-6(req13(o)-3(u)-3(e)9(n148(c)-C82)]



- 1. VBUS source identified (through PS detection and OTG pin)
- 2. VBUS power source good
- 3. VBUS above battery (not in sleep)
- 4. VBUS removed or below VACOV threshold
- 5. VBUS above V_{VBUSMIN} (typical 3.8V) (not a poor source)
- 6. Charge Complete
- 7. Any fault event in REG0C

When a fault occurs, OZ1C82 sends out IRQ and keeps the fault state in REG0C until the host reads REG0C. Before the host reads REG0C and all the faults are cleared, OZ1C82 wouldn't send any IRQ upon new faults. To read the current fault status, the host has to read REG0C twice consecutively. The 1st read reports the pre-existing fault status and the 2nd read reports the current fault status.

Safety Timer

If the safety timer is expired, the switch between VSYS and VBAT is off to prevent further charging, and LED blinks on and off with 1Hz frequency. The buck converter keeps enabled to supply system. CHRG_FAULT bits set to 11 and IRQ will generate 250µs low pulse. In charging mode, fast charging safety timer is programmed by REG07 [2:1], wake up timer is default 4hours. The safety timer can be disabled by setting EN_TIMER=0

During input voltage, current or thermal regulation, the safety timer counts at half clock rate because the real charge current could be lower than the register setting. This half clock rate feature can be disabled by setting EN_TMR2X=0

VBUS OVP (ACOV)

When VBUS voltage exceeds V_{ACOV} , OZ1C82 will stop switching immediately. During ACOV, the fault register CHRG_FAULT bits set to 01 and an IRQ asserts to the host.

System OVP

When over voltage happens for system, both buck converter and BATFET between VSYS and VBAT are off. The charging will be automatically restarted when OVP condition disappears.

System OCP

When the system is shorted or significantly overloaded ($I_{BAT}>I_{BATOP}$) so that its current exceeds the over-current limit, OZ1C82 latches off BATFET. BATFET Enable Section (Exit shipping mode) can reset the latch-off condition and turn on BATFET.

Thermal Protection in Buck Mode

OZ1C82 monitors the internal junction temperature T_J to avoid overheat and limits IC surface temperature in buck mode. When T_J exceeds the preset thermal regulation limit by TREG bits (REG08[1:0]), the charge current would be

lowered down. During thermal regulation, the actual charging current is usually below the setting charging current. So termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

OZ1C82 has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds $T_{\text{SHUT}}.$ The fault register CHRG_FAULT is set to 10 and IRQ is asserted to the host. The converter and BATFET will be enabled to recover when IC temperature lower than $T_{\text{SHUT HYST}}.$

Battery Overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charging function is disabled immediately. And the fault register BAT_FAULT bit goes high.

Battery Over-Discharge Protection

When battery is discharged below V_{BAT_DPL} , BATFET will be turned off to protect battery from over discharge. Battery will recover to be normal when an input source detected at VBUS. When an input source is plugged in, BATFET turns on, and the battery is charged with I_{SHORT} (typical 100mA) current when V_{BAT}
 $V_{BATSHORT}$, or pre-charge current as set in IPRECHG register when the battery voltage is between $V_{BATSHORT}$ and $V_{BATLOWV}$.

Battery Monitor

OZ1C82 can report V_{VBUS} , V_{BAT} , V_{SYS} , thermistor ratio, and charging current in battery monitor registers (REG0E-REG12). The battery monitor can be configured as two conversion modes by CONV_RATE bit (REG02[6]): one-shot conversion (default) and 1 second continuous conversion.

For one-shot conversion (CONV_RATE=0), the CONV_START bit needs to be set 1 to start the conversion. And CONV_START bit is cleared by OZ1C82 when conversion is completed. The conversion result is ready after t_{CONV} (maximum 1 second)

For continuous conversion (CONV_MODE=1), the CONV_START needs to be set 1 to start the conversion. During active conversion, the CONV_START keeps 1 to indicate conversion is in progress. The battery monitor provides conversion result every 1 second automatically. The battery monitor exits continuous conversion mode when CONV_START is cleared.

BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, OZ1C82 can turn off BATFET by setting BATFET_DIS=1



so that the system voltage is zero to minimize the battery leakage current. And BATFET can turn off immediately or delay by t_{SM_DLY} as defined by BATFET_DLY bit.

BATFET Enable (Exit Shipping Mode)

BATFET can be enabled to restore system power by one of the following events:

- 1. Plug in adapter
- 2. Clear BATFET_DIS bit
- 3. Set REG_RST=1 to reset all the registers including BATFET DIS bit to default 0
- 4. A logic high to low transition on PB# with t_{SHIPMODE} deglitch time to enable BATFET to exit shipping mode

Standby Mode Charge

In standby mode, there is no I²C command to be sent by host when both VBUS and battery are active, PS and CE# are low active; in this case, OZ1C82 can also complete a charging cycle automatically with default charging parameters are listed in the following table.

Table 3: Default charger parameters

Standby mode	Default charging parameters
Charging Voltage	4.208V
Charging Current	2048A
Wake up Current	128mA
Termination current	256mA
Recharging threshold	100mV
Wake up timer	4 hours
CC Charge timer	12 hours
Wake up threshold	3V
V _{SYSMIN} threshold	3.5V

Anytime, host can access OZ1C82 and change the charger parameters by I²C according to customer's charging requirements



Constant Voltage and Constant Current Operation

As shown in Figure 5, the charger in OZ1C82 uses six error amplifiers: EA1 for the adapter current limitation, EA2 for charging voltage regulation, EA3 for charging current regulation, and EA4 for VBUS voltage regulation, EA5 for system voltage regulation, and EA6 for thermal regulation. The outputs of these four error amplifiers are tied to the COMP pin for compensation.

The output of the adapter current-sense amplifier is connected to the error amplifier EA1. EA1's output is connected to the COMP pin. Therefore, whenever the AC adapter current limit is exceeded, EA1 output will control the COMP voltage. The charger's duty cycle will be reduced until the total adapter current falls within its limit value.

In a constant current regulation operation, the error amplifier EA3 will control the COMP pin voltage. The circuit operates to regulate the charger output current according to the desired current setting by I^2C programming with $\pm 5\%$ accuracy.

In a constant voltage operation, the error amplifier, EA2 will control the COMP pin. The circuit operates to regulate the charger output voltage according to the desired voltage setting by I^2C programming with $\pm 0.5\%$ accuracy.

In a VBUS voltage regulation operation, the error amplifier, EA4 will control the COMP pin. The circuit operates to regulate the VBUS input voltage according to the VBUS VLMT voltage setting by I²C programming with ±3% accuracy.

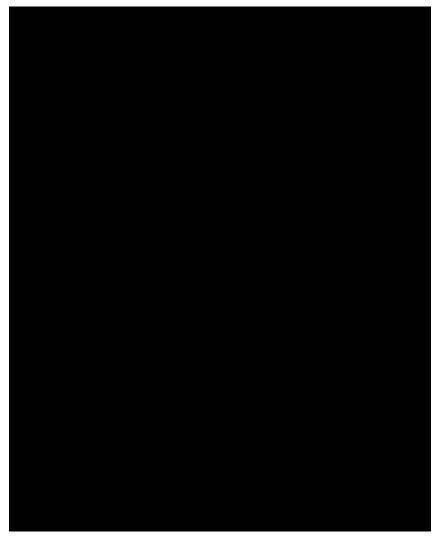


Figure 5: Voltage, Current and Thermal regulation loops

Serial Interface

The device uses I2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG14. Register read beyond REG14 (0x14) returns 0xFF. The I2C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

a) Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

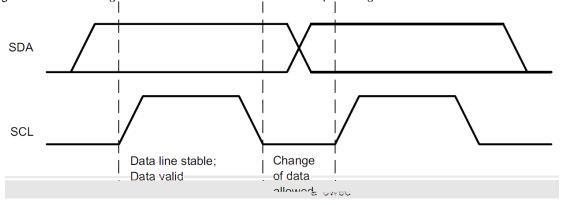


Figure 6: Bit Transfer on the I²C Bus

b) START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

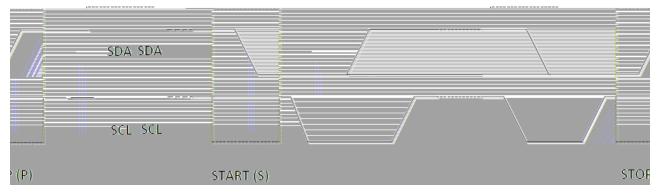


Figure 7: START and STOP conditions

c) Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

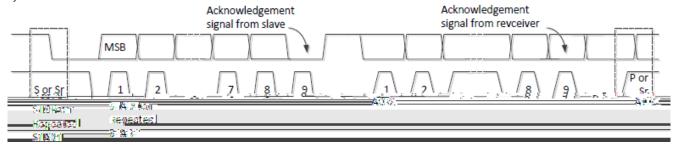


Figure 8: DATA Transfer on the I²C Bus

d) Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

e) Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

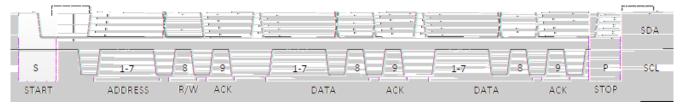


Figure 9: Complete Data Transfer

f) Single Read and Write

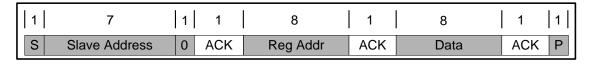


Figure 10: Single Write



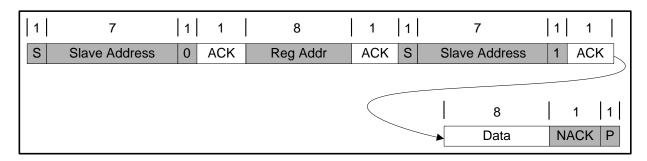


Figure 11: Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

g) Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG14 except REG0C.

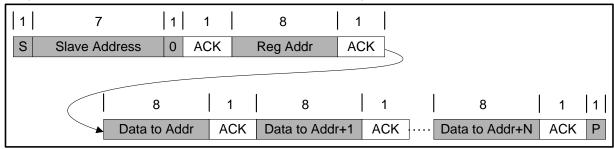


Figure 12: Multi-Write

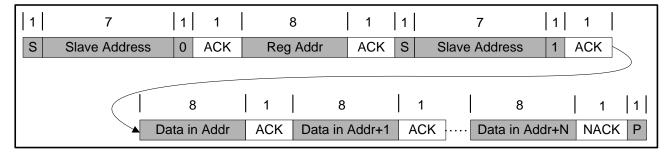


Figure 13: Multi-Read

REGOC is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REGOC reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REGOC for the second time. The only exception is NTC_FAULT which always reports the actual condition on the TS pin. In addition, REGOC does not support multi-read and multi-write.

Host mode and default mode

The OZ1C82 is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charge is in default mode, WATCHDOG_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG_FAULT bit is LOW.

After POR, the device starts in default mode with watchdog timer expired, or default mode, all the registers are in the default settings.

In default mode, the device keeps charging the battery with 12-hour fast charging safety timer. At the end of 12 hour, the charging is stopped and the buck converter continues to operate to supply system load. Any write command to the device will switch the default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WATCHDOG_RST bit before watchdog timer expires(WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits=00.

When the watchdog timer (WATCHDOG_FAULT bit=1) is expired, the device returns to default mode and all registers are reset to default value except IINLIM, VINDPM_OS, BATFET_RST_EN, BATFET_DLY and BATFET_DIS bits.

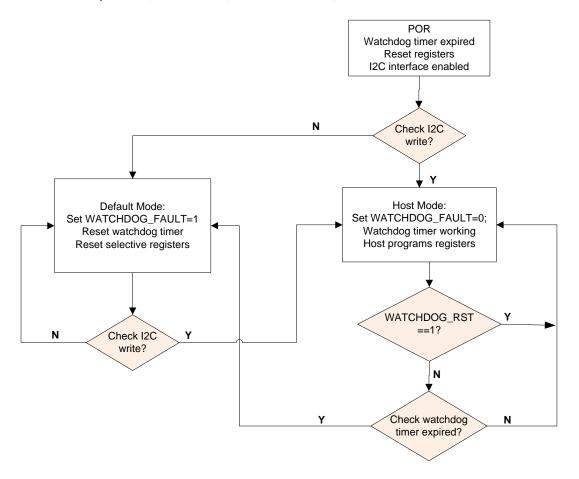


Figure 14: Watchdog timer for host mode and default mode



REGISTER MAP

Register index	Bit Number							
(hex)								
	EN_HIZ	EN_ILIM			IINI	_IM[5:0]		
	Reserved	Reserved	Reserved			VINDPM_OS[4:0]		
	CONV_START	CONV_RATE	Reserved	ICO_EN	Reserved	Reserved	FORCE_DPDM	AUTO_DPDM_EN
	BAT_LOADEN	WD_RST	Reserved	CHG_CONFIG		SYSMIN[2:0]		Reserved
	EN_PUMPX			•	ICHG[6:0]			
		IPREC	IPRECHG[3:0] ITERM[3:0]					
			VREG	G[5:0]			BATLOWV	VRECHG
	EN_TERM	Reserved	WATCH	WATCHDOG[1:0] EN_TIMER CHG_T		CHG_TI	MER[1:0] JEITA_ISE (0°C-10°C	
		BAT_COMP[2:0]			VCLAMP[2:0]		TRI	EG[1:0]
	FORCE_ICO	TMR2X_EN	BATFET_DIS	JEITA_VSET (45°C-60°C)	BATFET_DLY	BATFET_RST_EN	PUMPX_UP	PUMPX_DN
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		VBUS_STAT[2:0]		CHRG	_STAT	PG_STAT	Reserved	VSYS_STAT
	WATCHDOG_ FAULT	Reserved	CHRG_	FAULT	BAT_FAULT		NTC_FAULT[2:0]	•
	FORCE_VINDPM				VINDPM[6:0]			
	THERM_STAT				BATV[6:0]			
	Reserved				SYSV[6:0]			
	Reserved				TSPCT[6:0]			
	VBUS_GD				VBUSV[6:0]			



DETAILED REGISTER INFORMATION

This part describes the register definition and configuration for OZ1C82.

The following describes the register definition and configuration for charger module. Its I^2C slave write address is **D6H** and the slave read address is **D7H**.

	7	BN_HIZ	R/W	By REG_RST	0	Enable HIZ	
	<i>'</i>	U 1_1 112	14 44	By Watchdog	U	0v Disable	e(default) 1v Enable
	6	EN_ILIM	R/W	By REG_RST	1	Enable ILIN	M Pin
	0	LIV_ILIIVI	14 44	By Watchdog	ı	0v Disable	e 1v Enable(default)
	5	IIN⊔M[5]	R/W	By REG_RST	0	1600mA	Input Current Limit
	4	IINLIM[4]	R/W	By REG_RST	0	800mA	Offset:100mA
00	3	IINLIM[3]	R/W	By REG_RST	1	400mA	Range:100mA(000000)—3.25A(111111)
	2	IINLIM[2]	R/W	By REG_RST	0	200mA	Default:001000(500mA)
	1	IINLIM[1]	R/W	By REG_RST	0	100mA	(Actual input current limit is the lower of I2Cor ILIM pin)
							IINLIM bits are changed automatically after input source type
	0	IINLIM[0]	R/W	By REG_RST	0	50mA	detection is completed
	U						PSEL=Hi (USB500) = 500mA
							PSEL=Lo=3.25A
	7	Reserved	R	N/A		Always re	ads 0
	6	Reserved	R	N/A		Always rea	ads 0
	5	Reserved	R	N/A		Always rea	ads 0
	4	VINDPM_OS[4]	R/W	By REG_RST	0	1600mV	Input Voltage Limit Offset
	3	VINDPM_OS[3]	R/W		0	800mV	Default: 600mV (00110)
	2	VINDPM_OS[2]	R/W	By REG_RST	1	400mV	Range: 0mV—3100mV
	1	VINDPM_OS[1]	R/W	By REG_RST	1	200mV	Minimum VINDPM threshold is damped at 3.9V
							Maximum VINDPM threshold is damped at 15.3V
							When VBUSat no Load is ≤6V, the VINDPM_OSis used to
	0	VINDPM_OS[0]	R/W	By REG_RST	0	100mV	calculate VINDPM threshold
				, ,			When VBUSat no Load is > 6V, the VINDPM_OS multiple by 2 is
							used to calculate VINDPM threshold.

ADC Conversion Start Control

0—ADC conversion not active (default)

1—Start ADC Conversion

This bit is read-

7 CONV_START R/W By REG_RST By Watchdog



				D. DEC DET		Potton	and (IRATI OAD) Facilia	
	7	BATLOAD_EN	R/W	By REG_RST	0	Battery Load (IBATLOAD) Enable Ov Disabled (default) 1v Enabled		
				By Watchdog				
	6	WD_RST	R/W	By REG_RST	0		hdog Timer Reset	
	_		_	By Watchdog			nal (default) 1v Reset (Back to 0 after timer reset)	
	5	Reserved	R	N/A		Alwaysr		
	4	CHG_CONFIG	R/W	By REG_RST	1		Enable Configuration	
03		5. 15_55		By Watchdog		0v Char	ge Disable 1v Charge Enable(default)	
	3	SYS_MIN[2]	R/W	By REG_RST	1	0.4V		
				By Watchdog			Minimum System Voltage Limit	
	2	SYS_MIN[1]	R/W	By REG_RST	0	0.2V	Offset: 3.0V	
				By Watchdog	•		Range 3.0V-3.7V	
	1	SYS_MIN[0]	R/W	By REG_RST	1	0.1V	Default: 3.5V	
				By Watchdog				
	0	Reserved	R	N/A		Alwaysr	eads 0	
				By REG_RST			Pulse Control Enable	
	7	EN_PUMPX	R/W	By Watchdog	0		ole Current pulse control (default)	
				by waterledg		0—Enab	ole Current pulse control(PUMPX_UP and PUMPX_DN)	
	6	ICHG[6]	R/W	By REG_RST	0	4096mA		
	O	id iqoj	IV VV	By Watchdog	U	4030117		
	5	ICHG[5]	R/W	By REG_RST	1	2048mA		
	5	id id 3j	IV VV	By Watchdog	'	2040111	Fast Charge Current Limit	
	4	ICHCI 41	R/W	By REG_RST	0	1024mA	Offset:0mA	
	4	ICHG[4]	ry vv	By Watchdog	U	10241114	Range:0mA(0000000)—5056mA(1001111)	
	3	1CHG[3]	R/W	By REG_RST	0	512mA	Default:2048mA(0100000)	
	3	iunqoj	LX AA	By Watchdog	U	SIZIIIA	Note:	
	2	ICHG[2]	R/W	By REG_RST	0	OF Cros A	ICHG=0000000(0mA) disable charge	
	2		FV VV	By Watchdog	0	256mA	ICHG>1001111(5056mA) is damped to register value	
	1	ICIC(4)	R/W	By REG_RST	0	128mA	1001111(5056mA)	
	'	ICHG[1]	LX AA	By Watchdog	U	IZOIIIA		
	_	IC ICO	R/W	By REG RST	0	C 4 A		
	0	ICHG[0]	FV VV	By Watchdog	0	64mA		
	7	IDDECLICIO	R/W	By REG_RST	0	512mA		
	'	IPRECHG[3]	FV VV	By Watchdog	U	SIZIIA		
	_	IDDECLICEO	D/\\\	By REG_RST	_	0FC ^	Pre-charge Current Limit	
	6	IPRECHG[2]	R/W	By Watchdog	0	256mA	Offset:64mA	
	_	IDDECLIOUS	D/\^/	By REG_RST	_	400 ^	Range:64mA—1024mA	
	5	IPRECHG[1]	R/W	By Watchdog	0	128mA	Default:128mA (0001)	
		IDDEO IOCA	DOM	By REG_RST	,	04. 4	` '	
	4	IPRECHG[0]	R/W	By Watchdog	1	64mA		
	_	ITTO ALC:	DOM	By REG_RST	_	540 '		
	3	ITERM[3]	R/W	By Watchdog	0	512mA		
	_	ITTEN ALC:	D///	By REG_RST	_	056	Termination Current Limit	
	2	ITERM[2]	R/W	By Watchdog	0	256mA	Offset:64mA	
		17777 AT 43	D/A:	By REG_RST	_	400 .	Range:64mA—1024mA	
	1	ITERM[1]	R/W	By Watchdog	1	128mA	Default:256mA (0011)	
	_	ITTO ALC:	D/\4/	By REG_RST		04. 4		
	0	ITERM[0]	R/W	By Watchdog	1	64mA		
				. ,		4		



	7	VREG[5]	R/W	By REG_RST By Watchdog	0	512mV		
	6	VREG[4] R/W By REG_RST 1 256mV Charge Voltage Limit	Charge Voltage Limit Offset:3.84V					
	5	VREG[3]	R/W	By REG_RST By Watchdog	0	128mV	Range:3.84V—4.608V(110000)	
	4	VREG[2]	R/W	By REG_RST By Watchdog	1	64mV	Default:4.208V(010111) Note: VCHG>110000 (4.608V) is damped to register value 110000	
	3	VREG[1]	R/W	By REG_RST By Watchdog	1	32mV	(4.608V)	
	2	VREG[0]	R/W	By REG_RST By Watchdog	1	16mV		
	1	BATLOWV	R/W	By REG_RST By Watchdog	1	Battery Pre-charge to Fast Charge Threshold 0—2.8V 1—3.0V (default)		
•	0	VREOHG	R/W	By REG_RST By Watchdog	0 (/	Battery Recharge Threshold Offset (Below Charge Voltage Limit) 0-9-100mV (V _{RCHS}		



7	FORŒ_ICO	RW	By REG_RST By Watchdog	0	Force Start Input Ourrent Optimizer 0—Do not force ICO (default) 1—Force ICO Note: This bit is can only be set only and always return to 0 after ICO starts
6	TMR2X_EN	R/W	By REG_RST By Watchdog	1	Safety Timer Setting During DPM or Thermal Regulation 0—Safety time not slowed by 2X during DPM or thermal regulation 1—Safety time slowed by 2X during DPM or thermal regulation (default)
5	BATFET_DIS	R∕W	By REG_RST	0	Force BATFET off to enable ship mode 0—Allow BATFET turn on (default) 1—Force BATFET off
4	JETA_VSET (45°C—60°C)	R/W	By REG_RST By Watchdog	0	JETA High Temperature Voltage Setting 0—Setting charging voltage to VREG-200mV during JETA high temperature 1—Setting charging voltage to VREG during JETA high temperature
3	BATFET_DLY	R/W	By REG_RST	0	BATFET Turn Off Control 0—BATFET turn off immediately when BATFET_DISbit is set 1—BATFET turn off delay t _{SM_DLY} when BATFET_DISbit is set
2	BATFET_RST_ EN	R/W	By REG_RST	1 0—Disa	BATFET Full System Reset Enable 0—Disable BATFET full system reset 1—Enable BATFET full system reset
1	PUMPX_UP	₽₩	By REG_RST By Watchdog	0	Ourrent Pulse Control Voltage UP enable 0—Disable (default) 1—Enable Note: This bit can only be set when EN_PUMPX bit is set and return to 0 after current pulse control sequence is complete
0	PUMPX_DN	₽₩	By REG_RST By Watchdog	0	Ourrent Pulse Control Voltage Down enable 0—Disable (default) 1—Enable Note: This bit can only be set when EN_PUMPX bit is set and return to 0 after current pulse control sequence is complete
7	Reserved	R	N/A		Always reads 0
6	Reserved	R	N/A		Always reads 0
5	Reserved	R	N/A		Always reads 0
4	Reserved	R	N/A N/A		Always reads 0
3	Reserved	R			Always reads 0
1	Reserved Reserved	R R	N/A N/A		Always reads 0
0	Reserved	R	N/A		Always reads 0 Always reads 0
J	rxeservea	I.V.	IVA	I	/ niways i caus U



7	VBUS_STAT[2]	R	N/A	N/A	VBUSStatues Register
6	VBUS_STAT[1]	R	N/A	N/A	000: No Input
U	VDOS_SIAI[1]	IV.	1 1 1 1 1	IW A	001:USB Host SDP
					010:Adapter (3.25A)
5	VBUS_STAT[0]	R	N/A	N/A	111:OTG
					Note: Software current limit is reported in IINLIM register
4	CHRG_STAT[1]	R	N/A	N/A	Charging Status
<u> </u>	5: 3: 10_0:: 1.[1]				00—Not charging
		_			01—Pre-charge (<v<sub>BAπ.ow)</v<sub>
3	CHRG_STAT[0]	R	N/A	N/A	10—Fast charging
					11—Charge Termination Done
					Power Good Status
2	PG STAT	R	N/A	N/A	0—Not Power good
_			'7'		1—Power good
1	Reserved	R	N/A	0	Always reads 0
-	. 200. 100			Ť	VSYS Regulation Status
0	VSYS_STAT	R	N/A	N/A	0—Not in VSYS_MIN regulation
			'7'		1—In VS/S MIN regulation
					- <u>-</u>
					Watchdog Fault Satus
7	WATCHDOG_	R	N/A	1	0—Normal
	FAULT			-	1—Watchdog timer expiration (default)
6	Reserved	R	N/A	N/A	Always reads 0
5	CHRG_FAULT[1]	R	N/A	N/A	Charge Fault Status
					00—Normal
	O IDO FALILITA	_	N/ A	N1/ A	01—Input fault (VBUS-V _{ACOV} or VBAT <vbus-v<sub>VBUSMIN (typical 3.8V)</vbus-v<sub>
4	CHRG_FAULT[0]	R	N/A	N/A	10—Thermal shut down
					11—Charge safety timer expiration
2		_	NI/ A	NI/ A	Battery Fault Status
3	BAT_FAULT	R	N/A	N/A	0—Normal 1—BATOVP (V _{BAT} >V _{BATOVP})
2	NTC_FAULT[2]	R	N/A	N/A	NTCFault Status
1	NTC_FAULT[1]	R	N/A	N/A	Buck Mode:
					000—Normal
					010—THM warm
0	NTC_FAULT[0]	R	N/A	N/A	011—THM cool
					101—THM ∞ld
					110—THM hot
					VINDPM Threshold Setting Method
7	FORCE_VINDPM	R/W	By REG_RST	0	0—Run relative VINDPM threshold (default)
					1—Run absolute VINDPM threshold
6	VINDPM[6]	R/W	By REG_RST	0	6400mV Absolute VINDPM threshold
5	VINDPM[5]	R/W	By REG_RST	0	3200mV Offset: 2.6V
4	VINDPM[4]	R/W	By REG_RST	1	1600mV Range:3.9V(0001101)—15.3V(1111111)
3	VINDPM[3]	R/W	By REG_RST	0	800mV Note:
2	VINDPM[2]	R/W	By REG_RST	0	400mV Value<0001101 is clamped to 3.9V
1	VINDPM[1]	R/W	By REG_RST	1	200mV Register is read only when FORCE_VINDPM=0 and can be
_	\	D() 4 /	D . DEC . 2011	_	written by internal control based on relative VINDPM threshold
0	VINDPM[0]	R/W	By REG_RST	0	100mV setting
					Register can be read/write when FORCE_VINDPM=1



						Thermal P	legulation Status
	7	THERM_STAT	R	N/A	N/A	0—Norma	•
	,	INERVI_SIAI	K	IVA	IWA		mal regulation
	6	BATV[6]	R	N/A	0	1—In ther	mai regulation
	5		R	N/A	0	640mV	
	4	BATV[5]	R	N/A	0	320mV	ADC Conversion of Battery Voltage (V _{BAT})
		BATV[4]		N/A	0	160mV	Offset:2.304V
	2	BATV[3]	R R	N/A	0	80mV	Range: 2.304V(0000000) — 4.848V(1111111)
		BATV[2]		N/A		40mV	Default:2.304V(0000000)
	1	BATV[1]	R	N/A	0		
	0	BATV[0]	R	IVA	0	20mV	
	7	Reserved	R	N/A	0	Always rea	ads ()
	6	VSYS[6]	R	NA	0	1280mV	
	5	VSYS[5]	R	N/A	0	640mV	†
	4	VSYS[4]	R	N/A	0	320mV	ADC Conversion of System Voltage (V _{SrS})
	3	VSYS[3]	R	NA	0	160mV	Offset:2.304V
	2	VSY[2]	R	N/A	0	80mV	Range:2.304V(0000000)—4.848V(1111111)
	1	VSYS[1]	R	N/A	0	40mV	Default:2.304V(0000000)
	0	VSYS[0]	R	N/A	0	20mV	1
		र ा ज्ज	1	1470		Zomv	
	7	Reserved	R	NΑ	0	Alwaysrea	ads 0
	6	TSPCT[6]	R	NΑ	0	29.76%	
	5	TSPCT[5]	R	NΑ	0	14.88%	
	4	TSPCT[4]	R	N/A	0	7.44%	ADC Conversion of THM Voltage (V _{THM}) as Percentage of V _{LDO}
	3	TSPCT[3]	R	ΝA	0	3.72%	Offset:21%
	2	TSPCT[2]	R	NΑ	0	1.86%	Range:21%(0000000)—80%(1111111)
	1	TSPCT[1]	R	N/A	0	0.93%	Default:21%(0000000)
	0	TSPCT[0]	R	N/A	0	0.465%	
						VBUSGoo	d Status
	7	VBUS GD	R	N/A	N/A	0—Not VE	BUSAttached
	,	VBUS_GD	K	IVA	IWA	1-VBUS/	Attached
						VBUS_GD	
	6	VBUS[6]	R	N/A	0	6400mV	
	5	VBUS[5]	R	N/A	0	3200mV	ADC conversion of \/DLIC\/elters
	4	VBUS[4]	R	N/A	0	1600mV	ADC conversion of VBUS Voltage
	3	VBUS[3]	R	N/A	0	800mV	Offset: 2.6V
	2	VBUS[2]	R	N/A	0	400mV	Range: 2.6V (0000000) t 15.3V (1111111) Default: 2.6V
	1	VBUS[1]	R	N/A	0	200mV	DGIAUIT. 2.UV
	0	VBUS[0]	R	N/A	0	100mV	
_							
	7	Unused	R	N/A	0	Always Re	ads 0
	6	ICHGR[6]	R	N/A	0	3200mA	ADC Conversion of Charge Current (IBAT) when VBAT>VBATSHORT
	5	ICHGR[5]	R	N/A	0	1600mA	Offset:0mA
	4	ICHGR[4]	R	N/A	0	800mA	Range:0mA(0000000)—6350mA(1111111)
	3	ICHGR[3]	R	N/A		0 400mA	Default:0mA(0000000)
	2	ICHGR[2]	R	N/A	0	200mA	Note:
	1	ICHGR[1]	R	N/A	0	100mA	This register returns 0000000 for V _{BAT} <v<sub>BATSHORT</v<sub>
1	0	ICHGR[0]	R	N/A	0	50mA	G



7	VDPM_STAT	R	N/A	N/A	VINDPM S 0—Not in 1—In VINI	VINDPM	
6	IDPM_STAT	R	N/A	N/A	0—Not in	IINDPM Status 0—Not in IINDPM 1—In IINDPM	
5	IDPM_LIM[5]	R	N/A	0	1600mA		
4	IDPM_LIM[4]	R	N/A	0	800mA	Input Current Limit in Effect while Input Current Optimizer	
3	IDPM_LIM[3]	R	N/A	0	400mA	(ICO) is enabled	
2	IDPM_LIM[2]	R	N/A	0	200mA	Offset:100mA	
1	IDPM_LIM[1]	R	N/A	0	100mA	Range:100mA(000000)—3.25A(111111)	
0	IDPM_LIM[0]	R	N/A	0	50mA		
7	REG_RST	RW	N/A	0	Register Reset 0—Keep current register setting 1—Reset to default register value and reset safety timer Note: Reset to 0 after register reset is completed		

6 ICO_OPTIMIZED R N/A N/A

■ TYPICAL APPLICATION SCHEMTAIC

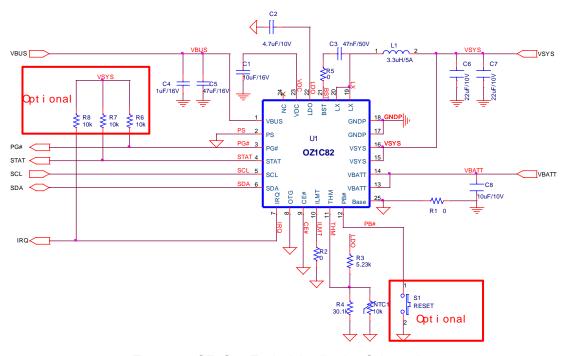


Figure 15: OZ1C82 Typical Application Schematic

BILL OF MATERIALS

Item	Qty	Reference	Value	Vendor	Part Number	PCB Footprint
1	1	C1	10μF/16V	Any	Ceramic – X7R or X5R	0805
2	1	C2	4.7μF/10V	Any	Ceramic – X7R or X5R	0805
3	1	C3	47nF/50V	Any	Ceramic – X7R or X5R	0603
4	1	C4	1µF/16V	Any	Ceramic – X7R or X5R	0603
5	1	C5	47µF/16V	Any	Ceramic – X7R or X5R	0805
6	2	C6,C7	22µF/10V	Any	Ceramic – X7R or X5R	0805
7	1	C8	10μF/10V	Any	Ceramic – X7R or X5R	0805
8	2	R1,R2	0Ω	Any	-	0603
9	1	R3	5.23kΩ 1%	Any	-	0603
10	1	R4	30.1kΩ1%	Any	-	0603
11	1	R5	Ω0	Any	-	0603
12	3	R6,R7,R8	10kΩ	Any	-	0603
13	1	NTC	103AT	-	-	0603
14	1	L1	3.3µH/5A	Würth Elektronik	74437346033	7.3x6.6x2.8
15	1	U1	-	O2Micro, Inc.	OZ1C82	QFN24 4mmx4mm



COMPONENT SUPPLIERS

Mamufacturer	Contact Information						
Manufacturer	Phone	Website					
Inductors							
Würth Elektronik	+49 (0) 79 42 945 -5000	http://www.we-online.com					
Capacitors							
Vishay	1-847-803-6100	www.vishay.com					
Johanson Dielectrics	1-818-364-9800	www.johansondielectrics.com					
TDK	1-800-344-2112	www.tdk.com					
SANYO	N/A	http://www.sanyo.com/components/					
Würth Elektronik	+49 (0) 79 42 945 -5000	http://www.we-online.com					
Resistors							
Vishay	1-402-563-6866	www.vishay.com					
TDK	1-800-344-2112	www.tdk.com					



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